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(54) Microstructure control of copper interconnects

(57) A method and structure is described which substantially eliminates the grain growth of copper due to self annealing. Basically, by alloying the copper interconnect e.g. with Cr, Co, Zn or Ag in an amount which does not cause a second phase or precipitation at the annealing temperature, one can control and maintain the grain size of the copper and hence achieve a uniform microstructure while improving the strength, hardness and CMP removal rate of the interconnect while substantially maintaining the conductivity of the copper.

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Description**Field Of The Invention**

[0001] This invention relates to integrated circuits employing copper interconnects and more particularly to the control of the copper interconnect microstructure to obtain improved interconnects.

Description Of The Related Art

[0002] A major limiting factor in ULSI interconnect technology is RC time delay introduced by the coupling of metal-insulator characteristics. An efficient interconnection scheme for advanced ULSI circuits requires materials with low effective time constants. In this regard, metals with low resistivity such as copper and the noble metals are emerging as materials of choice.

[0003] Some of the issues to be addressed in order for Cu-based interconnects to be a viable choice, especially as integration density continues to rise, involves the processes for patterning the copper lines, the prevention of diffusion of the copper into the underlying active substrate, the prevention of air corrosion on the surface of the copper and the uniformity of the microstructure of the copper. The issue of controlling and obtaining uniformity of the microstructure of the electroplated copper is addressed herein.

[0004] A more detailed background of the art regarding copper interconnects can be found with reference to the following publications which are incorporated herein by reference: R. L. Jackson, et al., "Processing and integration of copper interconnects", *Solid State Technology*, 49-59, March 1998; X W. Lin et al., "Future interconnect technologies and copper metallization", *Solid State Technology*, 63-79, October 1998; and P. Singer, "Tantalum, Copper and Damascene: The Future of Interconnects", *Semiconductor International*, 91-98, June 1998.

[0005] Also, one may refer to The Metals Handbook, 8th Edition, Vol. 1, page 802, "Properties and Selection of Metals", wherein various alloys of copper are discussed with respect to their physical and electrical properties and uses, including uses in connectors and sliding contacts, and which is incorporated herein by reference. It may be noted that there is no mention of the use of such alloys in IC's, nor of the self annealing problem of copper interconnects in IC's.

[0006] The recrystallization of electrodeposited copper due to self annealing and subsequent device processing which changes the mechanical and metallurgical properties of the copper requires a thorough understanding of microstructure control. If structural/property relationships and effects of annealing parameters are not well understood and controlled, a non-homogeneous microstructure can result which may lead to lower mechanical and electrical reliability of the finished integrated circuit device. Copper films have a

tendency to self anneal over time. During this self annealing process, copper atoms migrate and cause the grain size of the microstructure to grow. This growth in grain size reduces sheet resistance and alters the mechanical properties of the film. Further, migration of copper atoms into underlying circuit elements e.g. the dielectric layers and/or the silicon are highly detrimental to device performance. It would therefore be desirable to control the copper microstructure to provide a uniform copper microstructure which is not substantially degraded by self annealing or during subsequent processing steps.

Summary Of The Invention

[0007] We now provide a method and structure to substantially eliminate the grain growth of copper due to self annealing. Basically, by properly alloying the copper interconnect, one can control and maintain the grain size of the copper and hence achieve a uniform microstructure while improving the strength, hardness and CMP removal rate of the interconnect while substantially maintaining the conductivity of the copper. Accordingly, the present invention is described as follows.

[0008] A method of making an integrated circuit having copper interconnects comprises alloying the copper of the interconnect with one or more elements which can control and maintain the grain size and grain boundaries of the copper, without significant loss of electrical properties, said alloying elements being present in an amount less than that which creates a second phase or precipitate within the alloy, at least at the annealing temperature.

[0009] The invention further includes the integrated circuit device having such alloyed copper interconnects.

Brief Description Of The Drawings**[0010]**

Figure 1 is a cross-sectional view of a portion of an integrated circuit device depicting a copper interconnect structure.

Detailed Description Of The Invention

[0011] Referring to the Figure, there is shown a copper interconnect structure in an integrated circuit. As shown, the device 10 comprises a silicon substrate 12, a metallization layer 14 over a portion of the substrate 12, a dielectric layer 16 having trenches, vias, damascene or dual damascene structures therein, the trenches or other structures being filled with a copper diffusion barrier layer 18, a copper seed layer 20 and a bulk copper interconnect 22. Typical dielectric layers 16 include silicon dioxide, tantalum oxide, low k dielectrics as are known in the art and polymeric xerogels and aerogels. Typical barrier layers 18 may be formed from

materials such as Ta, TaN, Ta/TaN, TaSiN, WN or WSiN by vapor deposition or other techniques known in the art. The barrier layer 18 is generally about 25 - 500 Å thick. The function of the barrier layer 18 is to prevent the detrimental migration of copper into the dielectric 16 and the silicon 12. It should be noted that the invention is not limited to any specific barrier layer or barrier layer thickness. Other barrier layers including mono-layer self-assembled films can also be employed.

[0012] The copper seed layer 20 may be formed by PVD or CVD techniques which are well known in the art to a thickness preferably of from 25 - 2,000 Å. In one embodiment of the present invention the copper alloying elements are added to the seed layer 20 during deposition thereof. Thereafter, the bulk copper interconnect 22 is formed by methods well known in the art. While we believe that the preferred method of depositing the bulk copper layer is by known electrodeposition techniques, preferably utilizing standard commercially available electrochemical copper plating baths, the invention is meant to include other methods of depositing the bulk copper layer as well, e.g. by chemical vapor deposition. Typical copper electroplating baths, which are available from companies such as Enthone, Shipley, Lea Ronal and others, are generally comprised of copper sulfate, sulphuric acid, EDTA and a surfactant. The alloying elements in the seed layer 20 are then preferably diffused into the electroplated copper interconnect using a relatively low temperature (100°C-400°C) anneal for 1 - 3 hours in either a reducing gas, e.g. forming gas, or inert gas, e.g. N₂ or Argon atmosphere to cause the dopant to migrate to the grain boundaries of the electro-deposited copper and pin those boundaries so as to substantially prevent grain growth over time by self annealing. The dopant concentration should be below the solubility limit of the dopant in the copper at the annealing temperature.

[0013] Suitable alloying elements include Cr, Co, Zn and Ag. However, any element which would pin the grain boundaries without substantially adversely affecting the conductivity of the copper and without forming a second phase or precipitate at the annealing temperature may be employed. Typically, the resultant concentration of these elements in the electroplated copper is about 0.5 wt % or less. The exact amount of alloying element employed can be tailored to obtain not only a desired uniform microstructure but to enhance such properties as the CMP etch rate, strength and hardness of the interconnect. However, the concentration of alloying element should not exceed that which would cause a second phase or precipitate to appear in the copper microstructure at least at the annealing temperature, and preferably even at room temperature. Subsequent to electrodeposition and annealing, the device is completed by well known techniques.

[0014] In another embodiment of the invention, one can add the alloying element as a soluble dopant in the electroplating solution. Still other embodiments include

using dopant-containing copper targets and sputter depositing the dopants utilizing such targets; alternately depositing thin layers of dopant/copper/dopant etc. to form the seed layer, followed by annealing as set forth above; or doping the barrier layer and annealing to allow the dopant to migrate in and through the seed layer into the bulk copper interconnect.

Claims

1. An integrated circuit device having copper interconnects said interconnects having one or more alloying elements therein which elements substantially prevent grain growth of the copper due to self annealing.
2. The device recited in claim 1 wherein the alloying elements comprise at least one member of the group consisting of Cr, Co, Zn and Ag.
3. The device recited in claim 1 wherein the alloying elements are present in an amount less than the solubility limit of the elements in copper at the annealing temperature employed to disperse said elements in the copper.
4. The device recited in claim 1 wherein the alloying elements do not create a second phase or precipitate within the alloy.
5. The device recited in claim 4 wherein the alloying elements do not comprise more than 0.5 wt.% of the copper.
6. The device recited in claim 1 further comprising a Si substrate, a dielectric layer over at least a portion of said substrate and having a trench, via, damascene or dual damascene structure therein, a Cu migration barrier layer in said trench, via or damascene structure, a Cu seed layer over said barrier layer and wherein said copper interconnect is electrodeposited to essentially fill the remainder of the trench, via or damascene structure.
7. The device recited in claim 6 wherein the dielectric layer is selected from the group consisting of silicon dioxide, tantalum oxide, a low k dielectric, a xerogel and an aerogel.
8. The device recited in claim 6 wherein the barrier layer is from 25 - 500 angstroms thick and the copper seed layer is from 25 - 2,000 angstroms thick.
9. A method of forming an integrated circuit device having copper interconnects which are not prone to grain growth due to self annealing comprising alloying the copper of the interconnect with one or more elements which can control and maintain the grain

size and grain boundaries of the copper without significant loss of conductivity, including the step of annealing, wherein the alloying elements are present in an amount less than that which creates a second copper phase or precipitate within the alloy 5 at the annealing temperature.

10. The method recited in claim 9 wherein the device structure comprises a Si substrate, a dielectric layer over at least a portion of said substrate and having 10 a trench, via, damascene or dual damascene structure therein, a Cu migration barrier layer in said trench, via or damascene structure, a Cu seed layer over said barrier layer and wherein said copper interconnect is electrodeposited to essentially fill 15 the remainder of the trench, via or damascene structure, and wherein alloying of the copper is accomplished by introducing the alloying elements to at least one of the following; the barrier layer, the seed layer; and the copper interconnect, and then 20 annealing the device to diffuse the alloying element throughout the copper interconnect.
11. The method recited in claim 10 wherein the alloying elements comprise at least one member of the 25 group consisting of Cr, Co, Zn and Ag.
12. The method recited in claim 10 wherein the alloying element is incorporated into the seed layer during formation of that layer by a PVD or CVD process. 30
13. The method recited in claim 12 wherein the seed layer is from 25 - 2,000 Å thick.
14. The method recited in claim 10 wherein the seed 35 layer is formed by forming alternate layers of copper and alloying element.
15. The method recited in claim 9 wherein annealing is at a temperature of from 100°C-400°C for 1 -3 40 hours in a reducing or inert atmosphere.

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FIG. 1

